Application No. 09/630,258
Filed: August 1, 2000
TC Art Unit: 2124
Confirmation No.: 7200

AMENDMENTS TO THE CLAIMS

1. (currently amended) A method ~~for~~ of computing a fast Fourier transform, the method comprising:

(a) receiving ~~a~~ N time-ordered first data values;

(b) sequentially storing in a first memory each of said N time-ordered first data values in the time-order;

(c) storing in a second memory a plurality of twiddle factors in a bit reversed order;

(d) reading R input butterfly data values of said N first data values, ~~where~~ wherein ~~each of~~ said R butterfly data values are separated by N/R first data values in said ~~plurality of~~N time-ordered first data values;

(e) performing a radix R butterfly calculation on said R butterfly input data using at least one of the plurality of twiddle factors stored in the second memory to generate R butterfly output data values;

(f) storing said R butterfly output data values in sequential memory locations of a third memory ~~in the order in which the output data values are used in the calculations in a next stage~~; and

(g) performing said steps (c) - (f) N/R x 2 times,

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wherein said reading step (d) includes reading the R butterfly data values from said third memory, and

wherein the memory store operation performed in said storing step (f) has a unity stride, thereby allowing R butterfly data values to be read from contiguous memory locations each time the R butterfly data values are read from said third memory.

2. (previously presented) The method as in claim 1 further comprising the steps of:

replacing said N first data values in said first memory with selected ones of said R butterfly output data stored in said third memory location;

repeating steps (c) - (g) a total of $\log_r(n)$ times.

3. (original) The method as in claim 1, wherein R=2.

4. (original) The method as in claim 1, wherein said R=4.

5. (currently amended) Apparatus for calculating a fast Fourier transform, the apparatus comprising:

a first processor stage having an output including:

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a first memory ~~containing~~ storing N time-ordered input data values, said N input data values being stored in said first memory sequentially in the time-order ~~of said N input data values;~~,

a second memory ~~containing~~ storing a plurality of twiddle factor values, said plurality of twiddle factor values being stored in said second memory in a bit-reversed order~~;~~,

a third memory ~~containing~~ storing a plurality of output data values~~;~~, and

a radix R fast Fourier transform calculator coupled to said first, second, and third memories, said radix R fast Fourier transform calculator being operative to receive ~~from said first memory,~~ R selected data values of said N input data values, ~~each of~~ the R data values being separated by N/R input data values, said radix R fast Fourier transform calculator ~~further~~ being further operative to receive at least one twiddle factor value from said second memory, and said radix R fast Fourier transform calculator ~~further~~ being further operative to calculate R output data values using the at least one twiddle factor value and to write said R output data values into sequential memory locations of said third memory; and

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a second processor stage coupled to said output of said first processor stage,

wherein ~~said R output data values are stored said third memory in the order said R output data values are used in the~~ calculations performed in said second processing stage include reading the R butterfly data values from said third memory, and

wherein the memory write operation performed by said radix R fast Fourier transform calculator into the sequential memory locations of said third memory has a unity stride, thereby allowing R butterfly data values to be read from contiguous memory each time the R butterfly data values are read from said third memory.

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6. (original) The apparatus of claim 5 wherein R equals 2.

7. (original) The apparatus of claim 5 wherein R equals 4.

8. (currently amended) Digital signal processing apparatus for performing a fast Fourier transform calculation, comprising:

a first processor stage having an output and including~~:~~

a digital signal processor operative to receive N time-ordered first data values~~;~~,

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said digital signal processor operative to sequentially store in a first memory each of said N first data values in the time-order~~,~~,

said digital signal processor operative to store in a second memory a plurality of twiddle factors ~~stored in sequential locations~~ in a bit reversed order;

said digital signal processor operative to read R input butterfly data values of said N first data values, ~~where~~ wherein ~~each of~~ said R input butterfly data values are separated by N/R data points in said ~~plurality of~~N time-ordered first data values~~,~~,

said digital signal processor operative to perform a radix R butterfly calculation on said R butterfly input data~~,~~,

said digital signal processor operative to provide R butterfly output data values using at least one of said plurality of twiddle factors~~,~~, and

said digital signal processor operative to sequentially store said R butterfly output data values in sequential memory locations of a third memory; and

a second processor stage having an input coupled to said output of said first processor stage,

wherein ~~said R butterfly output data values are stored in said sequential memory locations in said third memory in the order~~

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Application No. 09/630,258
Filed: August 1, 2000
TC Art Unit: 2124
Confirmation No.: 7200

~~said R butterfly output data values are used in the~~ calculations performed in said second processor stage include reading the R butterfly data values from said third memory, and

wherein the memory store operation performed by said digital signal processor in the sequential memory locations of said third memory has a unity stride, thereby allowing R butterfly data values to be read from contiguous memory locations each time the R butterfly data values are read from said third memory.

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